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PATENT APPLICATION
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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S): Dave Goh, et al.

CONFIRMATION NUMBER: 1530

SERIAL NO: 09/102,207 **GROUP ART UNIT:** 2652

FILED: June 22, 1998 **EXAMINER:** David Donald Davis

SUBJECT: WEB SERVER CHIP FOR NETWORK MANAGEABILITY

COMMISSIONER FOR PATENTS
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SIR:

APPEAL BRIEF

Appellant herein sets forth his reasons and arguments for appealing the Examiner's final rejection of claims in the above-identified case.

REAL PARTY IN INTEREST

This Patent Application has been assigned to Hewlett-Packard Development Company, LC, a Texas Limited Partnership having it principal place of business in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Appellant is aware of no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 41 are extant in the case.

Claims 31 through 41 have been withdrawn from consideration.

Claims 1 through 30 are rejected.

The appealed claims are claims 1 through 30.

STATUS OF AMENDMENTS

After the final rejection, Appellant filed a Response to Office Action dated August 7, 2003. In the Response to Office Action, no amendments were made to the claims.

SUMMARY OF THE INVENTION

Network management typically includes monitoring and controlling resources in computers. However, software for performing network management can be expensive to purchase and maintain. Agents within the network management use precious computational resources burdening a host computer. See the Specification at page 1, lines 6 through 31.

In one embodiment of the present invention, network management is accomplished with the use of a chip (38) for incorporation within a network device (18) that is connectable to a computer network (20,24,34). The network device (18) includes a host processor (40). See Figure 1 and the Specification at page 4, line 18 through page 5, line 2.

The chip (38) includes a media access controller (42), a host interface (52-54) and an embedded processor (48). The media access controller (42) is

connectable to the computer network (20,24,34). The media access controller (42) provides the chip (38) with access to the computer network (20,24,34) independent of the host processor (40). See Figure 3 and the Specification at page 7, line 23 through page 8, line 10.

The host interface (52-54) is connectable to the host processor (40). See Figure 3, and the Specification at page 8, line 22 through page 10 line 4.

The embedded processor (48) is coupled between the host interface (52-54) and the media access controller (42). The embedded processor (48) is programmable to function as a manageability web server, communicate with the host interface (52-54) and obtain manageability information about the network device (18). The embedded processor (48) is also programmable to send the manageability information to the media access controller (42) for transmission over the computer network (20,24,34). In this way, the chip (38) performs network management functions independent of the host processor (40). See Figure 3 and the Specification at page 11, line 12 through page 12, line 3.

For example, the network device (18) includes interchip communications means (70), a compliant device (74), a chip (38) and non-volatile memory (68). The compliant device (74) is coupled to the interchip communications means (70). See Figure 3 and the Specification at page 12, line 24 through page 13, line 5.

For example, the embedded processor (48) is coupled to the media access controller (42) and programmed to function as an HTTP

manageability web server. See the Specification at page 12, lines 4 through 12.

The network manager (30) is coupled to the computer network (20,24,34). The network manager (30) includes a web browser and a plurality of HTML files for instructing the network manager (30) to communicate with the embedded processor (48) in the network device (18) and perform network management of the network device (18). In this way, the embedded processor (48) can communicate with the network manager (30) independent of the host processor (40). See the Specification at page 11, lines 12 through 23.

ISSUES PRESENTED FOR REVIEW

The following issues are presented for review:

(1) whether under 35 U.S.C. § 102 (e) claims 1 through 3, 5 through 15, and 21 through 30 are anticipated by USPN 6,400,715 (*Beaudoin*).

(2) whether under 35 U.S.C. § 103 (a) claims 4 and 16 through 18 are unpatentable over *Beaudoin* in view of USPN 5,903,737 (*Han*).

(3) whether under 35 U.S.C. § 103 (a) claims 19 and 20 are unpatentable over *Beaudoin*.

GROUPING OF CLAIMS

The claims (1 through 3, 5 through 15, and 21 through 30) rejected under 35 U.S.C. § 102(e) do not stand or fall together. The claims 1 through 3, 5 through 15, and 21 through 30 are divided into three groups. The first group

contains claims 1 through 3 and 5 through 12. The second group contains claims 13 through 15. The third group contains claims 23 through 30.

In the argument section below, Appellant points out why the claims of each group are separately patentable. In short, each of the groups include an independent claim that sets out a different combination of elements than the independent claims in the other groups. Each of the independent claims sets out subject matter that is patentable over the cited art. Each group of claims is therefore separately patentable over the cited prior art.

ARGUMENT

Rejection of Claims under 35 U.S.C. § 102(e)

A. Overview Specifying Errors in the Rejection of the Claims

The criteria for a rejection under 35 U.S.C. § 102 has been clearly defined by the courts and confirmed by the U.S. Patent and Trademark Office. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner has failed to show that each and every element set forth in the claims is found either expressly or inherently in Beaudoin.

Below, Appellant clearly and unambiguously points out subject matter within each independent claim that is not disclosed or suggested by

Beaudoin. On the basis of this, Appellant believes all the claims are patentable over Beaudoin.

B. Description of *Beaudoin*

Beaudoin discloses a network address matching circuit and method. A circuit 200, preferably implemented on a single chip, consists of Ethernet media access control (MAC) blocks 1201,1221,1241, a first-in first-out (FIFO) RAM block 1301, a DRAM interface block 1421, a queue manager block 1401, an address compare block 150, an EEPROM interface block 801, a network monitoring multiplexer (mux) block 1601, an LED interface block 1801, a DIO interface block 1701, an external address interface block 184 and network statistics block 1681. Each of the MACS 1201, 1221, 1241 is associated with a communications port 116,117,118 of the circuit 200; thus, the circuit 200 has fifteen available communications ports for use in a communications system of the present invention. See column 14, lines 47 through 65.

C. Discussion of Group 1 claims (claims 1 through 5)

1. Subject matter within independent claim 1 not disclosed by *Beaudoin*

Independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor. Beaudoin does not disclose an embedded processor as described in claim 1 of the present case.

Specifically, claim 1 sets out that an embedded processor is between the host interface and the media access controller. The embedded processor is

programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin.

2. Errors made by the Examiner in the stated rationale for the Rejection

The Examine has failed to correctly ascertain the disclosed subject matter of Beaudoin. This has led to an incorrect rejection of independent claim 1 over Beaudoin. Below, Appellant specifically responds to untenable arguments made by the Examiner.

a. Response to the Examiner's Argument that multiport, multipurpose network integrated circuit (chip) 200 of Beaudoin includes an embedded processor

The Examiner has asserted that multiport, multipurpose network integrated circuit (chip) 200 of Beaudoin includes an embedded processor.

> Specifically, the Examiner has argued as follows:
> If there is not need for external processor in Beaudoin, then an absence of an external processor indicates that Beaudoin discloses a processor on single chip 200...

See the Office Action dated July 1, 2003 at page 4, line 19 through page 5, line 2.

The Examiner's argument appears to be based on the statement by Beaudoin at column 15, lines 5 through 7: "More particularly, this

consolidation results in the elimination of the need for an external CPU to control, or coordinate control, of all these functions."

However, this statement in Beaudoin does not specifically state that multiport, multipurpose network integrated circuit (chip) 200 includes an embedded processor, but only indicates that there is no need for an external CPU to control or coordinate control of functions performed by multiport, multipurpose network integrated circuit (chip) 200.

The Examiner's argument that single chip 200 includes a processor is completely without support from Beaudoin.

For example, Figure 1 includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown.

Additionally, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57.

Thus, the Examiner's argument that multiport, multipurpose network integrated circuit (chip) 200 contains a processor/CPU appears to be directly contradicted by the subject matter disclosed by Beaudoin.

b. Response to the Examiner's Argument that certain functions in Beaudoin are not unlike the functionality of an embedded processor

The Examiner has additionally argued as follows:

> Further, Beaudoin states that control, logic and communications are performed by the processes in the single chip, which is not unlike the embedded processor claimed in the instant application.

See the Office Action dated July 1, 2003 at page 5, lines 2 through 4.

In reality, the functionality of the embedded processor set out in claim 1 of the present application is not at all similar to the control, logic and communications performed by the entities in the single chip multiport, multipurpose network integrated circuit (chip) 200.

Specifically, Claim 1 sets out functionality of the embedded processor. The embedded processor is programmable to function as a manageability web server and obtains manageability information about the network device.

This functionality is clearly not performed by any entity within single chip multiport, multipurpose network integrated circuit (chip) 200 disclosed in Beaudoin. No entity within single chip multiport, multipurpose network integrated circuit (chip) 200 is programmable to function as a manageability web server. No entity within single chip multiport, multipurpose network integrated circuit (chip) 200 obtains manageability information about the network device.

Further, the Examiner appears to be asserting an improper standard to determine whether a reference anticipates an element of a claim. The standard is not whether, in a vague way, functionality in a reference is "not unlike" an element of a claim. Rather, as set out above, the standard is as follows: "A claim is anticipated only if each and every element as set forth in

the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Clearly, the Examiner has failed to show either expressly or inherently, that single chip multiport, multipurpose network integrated circuit (chip) 200 discloses an embedded processor that functions as set out in claim 1.

c. Response to the Examiner's assumption that Beaudoin discloses a manageability web server

The Examiner has argued as follows:

> The manageability web server, as claimed, communicates with the host interface, the processor of Beaudoin shows this in the figure 1 by way of the bi-directional arrows pointing inside single chip 200 and outside single ship 200.

See the Office Action dated July 1, 2003 at page 5, lines 7 through 10.

In this statement, the Examiner assumes the existence of a manageability web server within single chip multiport, multipurpose network integrated circuit (chip) 200. However, it is impossible to determine what entity within single chip multiport, multipurpose network integrated circuit (chip) 200 the Examiner regards as functioning as a manageability web server.

The only clue the Examiner has given is that manageability web server is connected to a bi-directional arrow. However, in Figure 1, none of the

entities connected to a bi-directional arrow (MAC 120, 122, 124, FIFOs 130, queue manager 140, LED interface 182, EEPROM interface 80, DRAM controller 142, statistics RAM 168, DIO interface 170) function or is able to function as a manageability web server.

D. Discussion of Group 2 claims (claims 13 through 15)

1. Subject matter within independent claim 13 not disclosed by *Beaudoin*

Independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor. The embedded processor is not disclosed or suggested by Beaudoin

Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin.

2. Errors made by the Examiner in the stated rationale for the Rejection

As discussed more fully above, the Examiner has asserted that Circuit 200 of Beaudoin includes an embedded processor. However, Beaudoin nowhere states or shows Circuit 200 including an embedded processor.

Beaudoin only indicates that there is no need for an external CPU to control or coordinate control of functions performed by circuit 200.

As discussed above, Figure 1 includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown.

Also, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57.

Further, claim 13 does not merely state that the chip includes an embedded processor. Rather, claim 13 particularly points out various features of the embedded processor. Claim 13 indicates the embedded processor is instructed to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. As discussed more fully above, none of this functionality is disclosed or suggested by Beaudoin.

Further, nothing in Beaudoin could be take to infer, for example, that any embedded processor within circuit 200 would be programmable to

function as a manageability web server, as set out in claim 13 of the present application. Beaudoin does not even mention the web or the internet.

E. Discussion of Group 3 claims (claims 23 through 30)

1. Subject matter within independent claim 23 not disclosed by *Beaudoin*

Independent claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. Beaudoin does not disclose or suggest a chip including an embedded processor programmed to function as an HTTP manageability web server.

2. Errors made by the Examiner in the stated rationale for the Rejection

As discussed above, the Examiner has asserted that multiport, multipurpose network integrated circuit (chip) 200 of Beaudoin includes an embedded processor. However, Beaudoin nowhere states or otherwise indicates that circuit 200 includes an embedded processor. Figure 1 of Beaudoin includes a block diagram of multiport, multipurpose network integrated circuit (chip) 200. No processor or CPU is shown.

Also, Beaudoin very specifically states that it is an object of the invention not to utilize a processor or CPU when implementing the functionality of multiport, multipurpose network integrated circuit (chip) 200. Specifically, Beaudoin states the following: "It is an object of the present

invention to provide apparatus and methods for hardware control of network switching functions rather than CPU based control." See column 2, lines 55 through 57.

Claim 23 particularly points out various features of the embedded processor. None of this functionality is disclosed or suggested by Beaudoin. Claim 23 indicates the embedded processor is programmed to function as an HTTP manageability web server. This functionality is disclosed or suggested by Beaudoin. Nothing in Beaudoin could be taken to infer that any embedded processor within circuit 200 is programmed to function as an HTTP manageability web server, as set out in claim 23 of the present application. Beaudoin does not even mention the web or the internet.

Rejection of Claims under 35 U.S.C. § 103(a)

A. Overview Specifying Errors in the Rejection of the Claims

The U.S. Patent and Trademark Office has set forth a methodology for establishing a *prima facie* case of obviousness. Specifically three basic criteria must be met.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

See MPEP 706.02 (j).

Appellant believes the Examiner has failed to establish a *prima facie* case of obviousness for the claims extant in the present case because there are claim limitations that are not taught or suggested by *Beaudoin* and/or *Han*.

B. Discussion of Claims 4 and 16 through 18

The Examiner has rejected claims 4 and 16 through 18 under 35 U.S.C. § 103 (a) as unpatentable over *Beaudoin* in view of USPN 5,903,737 (*Han*).

Beaudoin is discussed above. Han discloses an apparatus and method for serial data communication utilizing a general microcomputer.

Claims 4 and 16 through 18 are patentable based on the patentability of the underlying independent claims.

1. Claim 4

Claim 4 is patentable over Beaudoin and Han based on the subject matter set out in independent claim 1. As discussed above, independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor. Neither Beaudoin nor Han disclose an embedded processor as described in claim 1 of the present case.

Specifically, claim 1 sets out that an embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin or Han.

2. Claims 16 through 18

Claims 16 through 18 are patentable over Beaudoin and Han based on the subject matter set out in independent claim 13. As discussed above, independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor. The embedded processor is not disclosed or suggested by Beaudoin or Han.

Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin or Han.

C. Discussion of Claims 19 and 20

The Examiner has rejected claims 19 and 20 under 35 U.S.C. § 103 (a) as unpatentable over *Beaudoin*.

Claims 19 and 20 are patentable based on the patentability of underlying independent claim 13. As discussed above, independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and

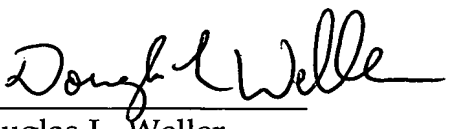
an embedded processor. The embedded processor is not disclosed or suggested by Beaudoin.

Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. As discussed above, none of this functionality is disclosed or suggested by Beaudoin.

CONCLUSION

For all the reasons discussed above, Appellant believes the rejection of the claims was in error and respectfully requests that the rejection be reversed.

Respectfully submitted,
DAVE GOH, ET AL.

By 
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Appendix: Appealed Claims

1. (Amended) A chip for incorporation within a network device connectable to a computer network, the network device including a host processor, the chip comprising:

a media access controller connectable to the computer network, the media access controller providing the chip with access to the computer network independent of the host processor;

a host interface connectable to the host processor; and

an embedded processor coupled between the host interface and the media access controller;

the embedded processor being programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device;

the embedded processor further being programmable to send the manageability information to the media access controller for transmission over the computer network;

whereby the chip performs network management functions independent of the host processor.

2. The chip of claim 1, wherein the embedded processor is programmable to obtain the manageability information in response to a network request addressed to the manageability web server.

3. The chip of claim 1, the network device further including an interchip communications means and a compliant device coupled to the interchip communication means, wherein the chip includes an interface connectable to the interchip communications means, and wherein the embedded processor is programmable to communicate via the interchip communication means interface to obtain manageability information about the compliant device.

4. The chip of claim 3, wherein the interchip communication means includes an I^2C bus, and wherein the compliant device is an I^2C-compliant device.

5. The chip of claim 3, wherein the embedded processor is also programmable to control the compliant device coupled to the interchip communications means.

6. The chip of claim 5, wherein the compliant device is a power supply controller, and wherein the embedded processor is programmable to control the power supply controller.

7. The chip of claim 5, wherein the compliant device is a fan controller, and wherein the embedded processor is programmable to control the fan controller.

8. The chip of claim 5, wherein the embedded processor is programmable to control the compliant device in response to a network request addressed to the manageability web server.

9. The chip of claim 5, wherein the embedded processor is programmable to perform firmware upgrades of the network device.

10. The chip of claim 1, wherein the embedded processor is programmable to perform network communications using TCP/IP.

11. The chip of claim 1, wherein the embedded processor is programmable to implement an HTTP web server.

12. The chip of claim 1, wherein the embedded processor is programmable to obtain manageability information from the host processor.

13. A network device connectable to a computer network, the network device comprising:

interchip communications means;

a compliant device coupled to the interchip communications means;

a chip including a media access controller connectable to the computer network; an interchip communications interface connected to the interchip communications means; and an embedded processor coupled to the interchip communications interface and the media access controller; and

non-volatile memory programmed with a plurality of executable instructions, the instructions, when executed, instructing the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network.

14. The network device of claim 13, wherein the instructions instructs the embedded processor to obtain the manageability information from the compliant device in response to network requests addressed to the manageability web server.

15. The network device of claim 13, further comprising a host processor; wherein the chip includes a host interface coupled to the host processor and the embedded processor and wherein the instructions instruct the embedded processor to obtain manageability information from the host processor.

16. The network device of claim 13, wherein the interchip communications means includes an I^2C bus, wherein the compliant device is an I^2C- compliant device, and wherein the instructions instruct the embedded processor to control the I^2C-compliant device in response to network requests addressed to the manageability web server.

17. The network device of claim 16, wherein the I^2C-compliant device is a power supply controller, and wherein the instructions instruct the embedded processor to control the power supply controller,

18. The network device of claim 16, wherein the I^2C-compliant device is a fan controller, and wherein the instructions instruct the embedded processor to control the fan controller.

19. The device of claim 13, wherein the non-volatile memory further stores web page content.

20. The device of claim 13, further comprising volatile memory for storing the manageability information.

21. The device of claim 13, wherein the instructions instruct the embedded processor to perform network communications using TCP/IP.

22. The device of claim 13, wherein the instructions instruct the embedded processor to implement an HTTP web server.

23. (Amended) A system (10) comprising:

a computer network;

a network device including a host processor and a chip, the chip including

a media access controller coupled to the computer network, and

an embedded processor coupled to the media access controller and programmed to function as an HTTP manageability web server; and

a network manager coupled to the computer network, the network manager including a web browser and a plurality of HTML files for instructing the network manager to communicate with the embedded processor in the network device and perform network management of the network device;

whereby the embedded processor can communicate with the network manager independent of the host processor.

24. The system (10) of claim 23, wherein the network device includes a compliant device and wherein the embedded processor is programmable to control the compliant device in response to control requests from the network manager.

25. The system (10) of claim 24, wherein the compliant device is a fan controller, and wherein the network manager can request the embedded processor to control the fan controller to adjust fan speed.

26. The system (10) of claim 24, wherein the compliant device is a power supply controller, and wherein the network manager can request the embedded processor to control the power supply controller to shut down and turn on the network device at scheduled times.

27. The system (10) of claim 24, wherein the compliant device is a power supply controller, and wherein the network manager can request the embedded processor to control the power supply controller to reboot the computer.

28. The system (10) of claim 24, wherein the network device further includes an upgradable BIOS; and wherein the network manager can send a BIOS upgrade program to the embedded processor and request the embedded processor to run the BIOS upgrade program.

29. The system (10) of claim 24, wherein the network manager can send a diagnostic program to the embedded processor and request the embedded processor to run the diagnostic program and return to the network manager results obtained by the diagnostic program.

30. The system (10) of claim 23, wherein the embedded processor is programmable to communicate with host interface and obtain manageability information from the host processor in response to requests by the network manager.